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| EXAMINER |
|---|
| HARKNESS, CHARLES A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 8 |

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/539,734 | HAMMARLUND ET AL. | |
| | Examiner | Art Unit | |
| | Charles A Harkness | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4-14, and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. In view of Applicant's amendment to the title, the previous objection has been withdrawn.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 9-11, 13-16, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrofer U.S. Patent Number 4,682,284 (herein referred to as Schrofer) in view of Joshi et al, U.S. Patent Number 5,954,815 (herein referred to as Joshi).

3. Referring to claims 1 and 21 Schrofer has taught a method including:

in a queue, writing a first object to a first location indicated by a write pointer (Schrofer column 3 lines 10-15);

making a qualitative determination whether or not to retain the first object within the queue based on the indicated invalidity of the first instruction (Schrofer column 3 lines 13-32);

if the qualitative determination is to retain the first object, then advancing the write pointer to indicate a second location within the queue into which to write a second object (Schrofer column 3 lines 10-32); and

if the qualitative determination is not to retain the first object, then maintaining the write pointer to indicate the first location within the queue into which to write the second object, so that the first object is overwritten by the second object (Schrofer column 3 lines 10-32). Schrofer has not explicitly taught where the object stored in the first location was an instruction. Schrofer has also not taught the plurality of instructions being written to the queue as a set of predetermined number of instructions, and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions.
Joshi has taught where the object stored in the first location was an instruction and where there is a plurality of instructions (Joshi abstract, figure 3, column 4 lines 12-15). Joshi has also taught the plurality of instructions being written to the queue as a set of predetermined number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions (Joshi column 7 lines 1-21; where the instructions that are after the delay instruction are indicated as being invalid, since they are outside of a trace of instructions; therefore if the first instruction comes after a delay instruction, it would be outside a specified trace, since it comes after a specified point, and then is considered to be invalid). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi. Both teach storing information into entries of a queue. One of ordinary skill in the art at the time of the invention would recognize that instructions could be stored in the queue of Schrofer after the

instructions have been fetched from an instruction cache (Joshi figure 3 reference number 50 column 4 lines 1-11). By fetching the maximum number of instructions before they are needed every time, which would make the number predetermined, and storing them in a queue allows the processor to have quick access to the instructions when it is ready to decode and/or execute the instructions. Now, when the processor is ready for the instructions, they are waiting in a queue in the processor and do not have to be fetched from some other memory, which delays the execution of that instruction. This is known as prefetching, and was a common method in the art at the time of the invention. Also, if the system does not want to execute certain instructions, for example if they follow a wrong branch prediction, then those instructions should be invalidated as taught in Joshi, so that the system does not waste clock cycles and time performing these operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi to reduce the access time needed to fetch instructions since the instructions are ready and waiting in a queue.

4. Referring to claim 13 Schrofer has taught an apparatus comprising:

a queue to buffer a first object propagated from a source to a destination (Schrofer column 3 lines 10-15); and

write logic to make a qualitative determination whether or not to retain the first object within the queue (Schrofer column 3 lines 13-16); if the qualitative determination is to retain the first instruction, to advance a write pointer to indicate a second location within the queue into which to write a second object; and, if the qualitative determination is not to retain the first object, to maintain the write pointer to indicate the first location within the queue into which to

write the second object, so that the first object is overwritten by the second object (Schrofer column 3 lines 10-32).

Schrofer has not explicitly taught where the object stored in the first location was an instruction. Schrofer has also not taught the plurality of instructions being written to the queue as a set of predetermined number of instructions, and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions.

Joshi has taught where the object stored in the first location was an instruction and where there is a plurality of instructions (Joshi abstract, figure 3, column 4 lines 12-15). Joshi has also taught the plurality of instructions being written to the queue as a set of predetermined number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions (Joshi column 7 lines 1-21; where the instructions that are after the delay instruction are indicated as being invalid, since they are outside of a trace of instructions; therefore if the first instruction comes after a delay instruction, it would be outside a specified trace, since it comes after a specified point, and then is considered to be invalid). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi. Both teach storing information into entries of a queue. One of ordinary skill in the art at the time of the invention would recognize that instructions could be stored in the queue of Schrofer after the instructions have been fetched from an instruction cache (Joshi figure 3 reference number 50

column 4 lines 1-11). By fetching the maximum number of instructions before they are needed every time, which would make the number predetermined, and storing them in a queue allows the processor to have quick access to the instructions when it is ready to decode and/or execute the instructions. Now, when the processor is ready for the instructions, they are waiting in a queue in the processor and do not have to be fetched from some other memory, which delays the execution of that instruction. This is known as prefetching, and was a common method in the art at the time of the invention. Also, if the system does not want to execute certain instructions, for example if they follow a wrong branch prediction, then those instructions should be invalidated as taught in Joshi, so that the system does not waste clock cycles and time performing these operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings taught by Schrofer and Joshi to reduce the access time needed to fetch instructions since the instructions are ready and waiting in a queue.

5. Referring to claims 2 and 14 Schrofer has taught wherein the qualitative determination includes examining a valid bit associated with the first instruction to determine validity of the first instruction (Schrofer figure 4 reference numbers 310,315, and 301 column 11 lines 16-25), making the qualitative determination to retain the first instruction if the valid bit indicates the first instruction is being valid, and making the qualitative determination not to retain the first instruction if the valid bit indicates the first instruction as being invalid (Schrofer column 3 lines 10-32).

6. Referring to claims 4 and 16 the combination of Schrofer and Joshi has taught wherein a plurality of instructions are written to the queue in a set of a predetermined number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions

that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, which is known beforehand, or predetermined), and wherein at least one instruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch instruction upstream of the at least one instruction in a stream of instructions (Joshi column 6 lines 35-53 and column 7 lines 1-21).

7. Referring to claim 9 the combination of Schrofer and Joshi has taught wherein the first instruction is received into the queue as part of a set of instructions comprising a first predetermined number of instructions and read from the queue to an instruction destination as part of a second set of instructions comprising a second number of instructions (Joshi column 4 lines 7-11 and line 51-column 5 line16; the number of instructions that are received by the queue is determined by how many instructions are dispatched each clock cycle, if no instructions are dispatched, then all four instructions are placed in the queue, and since different instructions are dispatched to different execution paths, shown in figure 3 reference numbers 74 and 82, instructions in some paths will take longer or shorter amounts of times, depending on the path it is in, therefore being part of different sets of instructions when it enters the queue and when it leaves the queue).

8. Referring to claims 10 and 20 Schrofer has taught wherein the first instruction is written from a source to a destination, and wherein the queue comprises a first path between source and destination, the method including propagating the first instruction from the source to the destination via a second path, not including the queue, if the queue is empty (Schrofer column 3 lines 40-58).

9. Referring to claim 11 Schrofer has taught including selecting between the first and second paths to receive the first instruction for propagation to the destination (Schrofer column 3 lines 40-58).

10. Referring to claim 22 Schrofer has taught wherein the sequence of instructions cause a multiprocessor to perform the step of examining a valid bit associated with the instruction to determine validity of the first instruction (Schrofer figure 4 reference numbers 310,315, and 301 column 11 lines 16-25), to make the qualitative determination to retain the first instruction if the valid bit indicates the first instruction as being valid, and to make the qualitative determination not to retain the first instruction if the valid bit indicates the first instruction as being invalid (Schrofer column 3 lines 10-32)..

11. Claims 5-8 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Schrofer and Joshi in further in view of Mitchell et al, U.S. Patent Number 4,841,476 (herein referred to as Mitchell).

12. Referring to claims 5 and 17 the combination of Schrofer and Joshi has not taught wherein the first instruction comprises a first microinstruction. Mitchell has taught wherein the first instruction comprises a first microinstruction (Mitchell figure 2, column 4 lines 35-39). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Mitchell. Microinstructions are used in many modern computers today, such as RISC systems. Microinstructions need to be stored in queues before, after, and/or during execution, just as any other instruction is stored so that the instructions are easily accessible with quick access time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the

invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Mitchell so that the microinstructions can be accessed by various parts of the processor from queues with small access times, which reduce the time for execution.

13. Referring to claims 6 and 18 the combination of Schrofer, Joshi, and Mitchell has taught wherein the first microinstruction is written to the queue from a microinstruction cache (Mitchell figure 2, column 4 lines 35-39).

14. Referring to claims 7 and 19 the combination of Schrofer, Joshi, and Mitchell has taught wherein the first microinstruction is part of a trace of microinstructions received from the microinstruction cache (Joshi column 4 lines 7-11 and line 51-column 5 line16; Joshi teaches that several instructions are dispatched from the cache to the queue, as part of a trace).

15. Referring to claim 8 the combination of Schrofer, Joshi, Panwar, and Mitchell has taught wherein the first instruction is received from an instruction source operating in a first clocking domain into the queue and read from the queue to an instruction destination operating in a second clocking domain (Schrofer column 9 line 62-column 10 line 15; it is described here where the clock signal that writes information into the queue is at a different frequency than the clock signal that is used to read information out of the queue).

16. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Schrofer and Joshi in view of Nemirovsky et al, U.S. Patent Number 6,477,562 (herein referred to as Nemirovsky).

17. Referring to claim 12 the combination of Schrofer and Joshi has not taught wherein the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the

first location into which the first instruction is written is located in the first portion if the first instruction comprises part of the first thread. Nemirovsky has taught wherein the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which the first instruction is written is located in the first portion if the first instruction comprises part of the first thread (Nemirovsky column 6 line 65-column 7 line 11; since a single queue could be partitioned for separate threads, it would be inherent that if one partition was allocated for a particular thread, than an instruction pertaining to that thread would be placed in that partition, or portion). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the combination of Schrofer and Joshi with the teachings of Nemirovsky so that the queue would be partitioned for multithreaded processing. By having separate portions or partitions in the queue for different threads allows the scheduler that dedicates different resources to the individual threads to easily access the instructions from the individual threads. When the scheduler is to send an instruction from thread 2, for example, it may go to the first entry from the second portion of the queue to find the next instruction for that thread, instead of searching through all the instructions for the next instruction for the second thread, which would result in a longer delay. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have separate portions or partitions in the queue for individual threads to reduce the amount of time to find and access the next instruction to be processed from a particular thread.

***Response to Arguments***

18. Applicant's arguments filed 04/29/03, paper number 7, have been fully considered but they are not persuasive.

19. In the remarks, in regard to the rejection of claim 1, on page 10, Applicant argues in essence that:

"In contrast [to the disclosure of Joshi], claim 1 requires a first instruction that is indicated as being invalid on account of being outside a trace of instructions."

20. This is not found persuasive. In Joshi, when a first instruction follows a delay instruction, it would be outside of a certain trace, and thus marked invalid. Nowhere in the claims does the Applicant discuss how to distinguish the trace of instructions, and which instructions fall outside of that trace of instructions, but simply states that by being outside of that trace makes the instruction invalid. This is also true in Joshi when the instruction comes after a delay instruction. The instructions that come before the delay instruction and including the delay instruction would make up a trace of instructions, and those instructions following the delay instruction would not be a part of that trace of instructions.

21. The Applicant also discusses different embodiments taught be Joshi in the arguments. However, Applicant is reminded that in MPEP § 2111.03 it states using the language "including" and words synonymous to "including" are inclusive or open-ended and do not exclude additional, unrecited elements or method steps.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness
Examiner
Art Unit 2183
July 8, 2003

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